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# TRANSMITTAL FORM

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| | Application Number 09/692,422 | Patent No. 6,959,271 |
| | Filing Date: October 19, 2000 | Issued: October 25, 2005 |
| | First Named Inventor | Peter Bellam |
| | Art Unit | 2125 |
| | Examiner Name | Albert William Paladini |
| Total Number of Pages in This Submission | Attorney Docket Number | S1022.80545US00 |

## ENCLOSURES (*Check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [x] Request for Certificate of Correction
- [x] Certificate of Correction
- [x] Pages 7 and 17 of Apl as Filed
- [x] Cols. 4, 9 and 10 of U.S. Patent No. 6,959,271
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] After Allowance Communication to TC
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- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
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Remarks

Certificate
FEB 23 2006
of Correction

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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| Firm Name | WOLF, GREENFIELD & SACKS, P.C. | | |
| Signature | | | |
| Printed name | James H. Morris | | |
| Date | February 16, 2006 | Reg. No. | 34,681 |

**Certificate of Mailing Under 37 CFR 1.8(a)**

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Signature: Gail Driscoll (Gail Driscoll)

Docket No.: S1022.80545US00
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| Applicant: | Peter Bellam | | |
| Serial No.: | 09/692422 | Patent No.: | 6,959,271 |
| Filed: | October 19, 2000 | Issued: | October 25, 2005 |
| For: | A METHOD OF IDENTIFYING AN ACCURATE MODEL | | |
| Examiner: | Albert William Paladini | | |
| Art Unit: | 2125 | Confirmation No.: | 6731 |

**Certificate of Mailing Under 37 CFR 1.8(a)**
I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as First Class Mail, in an envelope addressed to: Attention: Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: February 16, 2006

Gail Driscoll

**REQUEST FOR CERTIFICATE OF CORRECTION**
**PURSUANT TO 37 CFR 1.322**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the Specification:

Column 4, line 24 should read:

--particular 'X' on an output can indicate that an error has occurred as the signal has-- as it appears on page 7, line 1 of the application as filed.

Column 9, line 46 should read:

--In the following, Rl can have a resistance of 100 Ohms, R2-- as it appears on page 17, line 9 of the application as filed.

In column 10, line 1 should read:

--have an approximate value of 100 k Ohms. The circuit 308 is-- as it appears on page 17, line 34.

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: February 16, 2006

Respectfully submitted,

By: _____

James H. Morris
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(Also Form PTO-1050)

# UNITED STATES PATENT AND TRADEMARK OFFICE
## CERTIFICATE OF CORRECTION



| | | |
|---|---|---|
| PATENT NO. | : | 6,959,271 B1 |
| APPLICATION NO. | : | 09/692422 |
| ISSUE DATE | : | October 25, 2005 |
| INVENTOR(S) | : | Peter Bellam |

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 4, line 24 should read:
particular 'X' on an output can indicate that an error has

Column 9, line 46 should read:

In the following, RI can have a resistance of 100 Ohms, R2

Col. 10, line 1 should read:
have an approximate value of 100 k Ohms. The circuit 308 is

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plurality of signals having at least one abstract data type level to provide a set of expected results; means for replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; means for resimulating the model with said expanded set; means for comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

## DESCRIPTION OF THE DRAWINGS

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

FIG. **1** illustrates an inverter logic gate;

FIG. **2** illustrates an inverter logic gate as modeled by an analog model;

FIG. **3** shows control circuitry for providing input signals to an analog simulation model;

FIG. **4** shows schematically apparatus for reducing the RC delay when testing tristate conditions;

FIG. **5** shows an AND gate; and

FIG. **6** shows a flow chart of a method embodying the present invention.

## DETAILED DESCRIPTION

VHDL can describe the behaviour and structure of electronic systems in general and is suited as a language to describe the structure and behaviour of digital electronic hardware designs ie hardware cells. A cell is typically a relatively small part of the overall circuit design. Such device design is described in the VHDL language using the concept of a design entity. Each design entity is divided into two parts, the entity declaration and the architecture body. The entity declaration describes the external interface or connections to the design entity. The architecture body represents the internal description of the design entity such as its structure, behaviour or both.

FIG. **1** illustrates an inverter (INV) gate and it will now be described in VHDL. Considering the INV gate as a single cell, a single input pin and single output pin are required. Power and ground pins are not required to be defined.

The code in which such an inverter gate would be described in VHDL is

```
1. /*VHDL code for INV gate*/
2. library IEEE
3. use IEEE.STD_LOGIC_1164.all;
4. entity INV is
5. port (
6. A: in STD_LOGIC;
7. F: out STD_LOGIC
8. );
9. end INV;
10. architecture VI of INV is
11. begin
12. F<=not (A) after T;
13. end VI
14. /*end of VHDL code
```

Line **1** is simply a comment which allows the user to make notes referring to the code as a memory aid. The /* and */ notation indicate the start of a comment and the end of the comment respectively. This instructs the compiler to ignore the line of VHDL as the first line does not contain instructions for the compiler.

Lines **2** and **3** are a library clause (library IEEE) and a use clause (use IEEE.STD_LOGIC_1164.all;) respectively. These provide the design entity INV with access to all the names declared in the package STD_LOGIC_1164 stored in the library IEEE and particularly in the data type STD-LOGIC.

The data type of a pin sets out the values of different signal strengths and signals which may flow through the pin.

VHDL supports many such data types which are of an abstract nature including unknowns and high impedance. In order to cater for such abstract values a standard, numbered 1164, has been adopted by the IEEE. This standard defines a standard package containing definitions for a standard 9 valued data type. The standard data type is called standard logic and the IEEE 1164 package is sometimes referred to as the standard logic package or MVL 9 (for multi-value logic **9** values). The standard also defines the logical operations for theses data types, for example the NOT operation.

Each of the nine states of the IEEE 1164 standard logic package are explained below.

'U':This represents a strong unknown, that is as an input a 'U' indicates anything from a strong low to a strong high. If a 'U' is an output nothing has modified the outputs.

'X':This also represents a strong unknown and can be anything from a strong low to a strong high signal. In articular 'X' on an output can indicate that an error has occurred as the signal has passed through the model.

'-':This also represents a strong unknown and as such can be anything from a strong low to a strong high signal. This is sometimes referred to as NOT 'X'. It can provide a good logic level but it is a don't care state where its actual value is unimportant.

'W':This state is a weak version of the 'X' data type noted above.

'L':This data type represents a weak low, that is a low signal having a weak drive strength. This state can also represent a charge storage when used as an output state.

'H':This is exactly the same as an 'L' however in the opposite sense, that is to say it represents a weak high.

'0':This is a strong low which can be input directly into a model.

'1':This is a strong high and is the same as a 0 but in the opposite sense.

'Z':This represents a high impedance signal and when used as an input it means nothing drives the node.

Referring back to the VHDL description of the invention, line **4** provides an arbitrary level to the design entity. This line starts the definition of a new VHDL design unit. Because the library and use clauses are written before the entity declaration they do not begin the VHDL description of the design unit, there are merely context clauses.

The entity declaration includes port declarations which are in lines **5** to **9**. Ports may be pins on ICs or any other edge connection on a board etc. Technically ports are signals and so signals and ports are read in the same way. The port declaration includes the name of each port, the direction in which information is allowed to flow through the ports and the data type of the ports as described above. The entity declaration is completed by the VHDL word "end". "A" is therefore an input and "F" an output.

The architecture body, which is in lines **10** to **13**, represents the internal behaviour and structure of the design entity and is itself given an arbitrary name, in this case V1. The VHDL word "begin" signifies the start of the architecture statement part. The next line, line **12**, is a concurrent signal assignment which describes how the design entity will actually function. This line of code is executed each time the input changes value after a time T which can be defined elsewhere. In the case of an inverter the output F is defined

The WIF2TB tool expands the stimulus and response levels into a realisable set for the ELDO simulator. The resultant test bench is a mix of voltage supplies and voltage controlled switches with varying ON resistances. Some pins can have very simple circuitry connected to them.

The program has three basic separate algorithms depending on the complexity of the required stimulus for each pin. This is done to reduce the time needed for simulation by using the simplest possible circuit for all cases. The first algorithm basically states that any pin that never changes can be tied off to one of the supplies by a required drive resistor. The second algorithm basically uses a pattern producing voltage supply and a resistor to model any two level stimulus of equal drive. That is any pin which is driven between 0 and 1. The third algorithm defines complex stimuli using voltage controlled switches using pattern producing voltage sources.

For any pin that always has the same state the test bench has written to it a single resistor connected to the relevant supply. If the pin is an input, the supply used is the true level of the pin. If the pin is an output then the voltage used is the voltage of the inverted logic state. The inversion is required to give the output something to drive against to prove its drive strength. Also in the case of an output, the drive strength is reduced.

Because of the algorithm used in expansions, this type of case only exists for pins that are held at or drive a strong 0 or 1. Any tie-offs declared in the input WIF file will also have the same kind of circuit used to give the effect. The following table gives all the possible cases for this type of situation:

TABLE T.1

| LEVEL | DIRECTION | RESISTOR USED | SUPPLY USED |
|---|---|---|---|
| Strong 0 | Input | R1 | GND |
| Strong 1 | Input | R1 | $V_{DD}$ |
| Strong 0 | Output/Bidirectional | R2 | $V_{DD}$ |
| Strong 1 | Output/Bidirectional | R2 | GND |

The resistors R1 have the lowest resistance and are used to drive strong signals. The resistors R2 are used for the strong edge of the weak drive strength band. The resistors R4 have the highest resistance and are used to produce the very weakest signals.

In the following, Rl can have a resistance of 1000 hms, R2 a resistance 100 K Ohms, R3 a resistance of 250 K Ohms and R4 a resistance of 1 MegaOhm. These values are by way of example only.

In FIG. **3**, resistor (R1) **302** is connected between high voltage supply rail VDD and the input to the analog model. This provides the strong 1 state to the analog model. Analogously resistor (R1) **303** is connected to the ground GND supply rail to supply strong 0 signals as inputs to the analog model. In this way inputs to the analog model which are identified as never changing state can be tied off to one of these inputs depending upon whether they are permanently strong high or low signals. This is provided by the first algorithm.

Resistor (R1) **304** is connected-between a control input port **306** and the input to the hardware cell **301**. By inputting a series of 0 and 1 signals as control signals on terminal **306** a series of strong 0 and 1 signals can be applied to the cell. This is provided by the second algorithm.

The following are used by the third algorithm. Signal generating circuits **308** and **309** each include a voltage control switch connected to a resistor R2. These resistors have an approximate value of 100 kohms. The circuit **308** is connected to the ground line whilst circuit **309** is connected to the high voltage supply line VDD. Each voltage controlled switch is operable in response to control signals input on control input terminals **310** and **311** respectively. The inputs on these terminals will be a series of 0's and 1's produced by the WIF2TB tool to control the operation of the circuits **308** and **309**. The outputs of these two circuits are connected to node **314** which is connected to an input of the hardware cell.

Output signal generating circuits **315** and **316** each include a respective resistive element R3 together with a respective voltage control switch. Circuitry **315** is connected to receive a high voltage signal VDD whilst circuitry **316** is connected to receive the ground signal GND. Control terminals **317** and **318** control the voltage controlled switches in the circuits **315** and **316** respectively. Once again the input signals on the control terminal **317** and **318** will be a series of 0's and 1's produced by the tool to control the output at node **314**. The circuitry **308, 309, 315** and **316** are used in the expansion of 'L' and 'H' states into an expanded package suitable for application to the inputs of the analog model of the hardware cell **301**.

As described above 'L' states are expanded into very weak low and strong weak low signals. These are provided from circuits **316** and **308** respectively under control of the signals applied to control terminals **318** and **310**.

H states are expanded into strong weak high signals and very weak high signals by circuitry **309** and **315** respectively.

Hence any input of the analog model which in the corresponding VHDL model has an L or H state applied to the input can be stimulated by the expanded logic package by applying very weak and strong weak signals to the input. Although node **314** is shown providing only one signal input into the cell **301** it will be understood that any number of inputs of the analog model could be connected to the node **314**.

As described hereinbefore some pins may be bidirectional so that it is unknown whether the pin is an input or an output. In order to deal with this situation such pins are input with stimulus having a weak drive strength. In this way strong outputs will override the input. The weak drive strengths are produced by utilising a high resistance element R4 as shown in output circuitry **320,321**. Each of these circuits comprises a resistive element R4 connected in series with a voltage controlled switch. Circuit **320** is connected to the ground rail whilst circuit **321** is connected to the high voltage supply VDD. The voltage control switches of each circuit is controlled by input signals input on terminals **322** and **323** respectively. The control signals input on these terminals will be a series of 1's which will operate to open and close the switches in the circuits **320,321** to thereby control the voltage on node **324**. The signal at node **324** is connected to the bidirectional pin inputs of the analog model of the hardware cell **301**.

Outputs of the analog model can be driven by resistive elements **326** and **327** which operate to provide varying drive strengths for the signals which are input on control terminals **328** and **329** respectively.

For any pin that has got a single drive strength and on which the signal alternates between high and low states a pattern producing voltage source is connected to the pin by the drive modelling resistor. Output pins are driven by the weaker inverted level. Outputs of the analog model are connected to resistive elements **326** and **327** which operate to provide varying drive strengths for the signals which are

particular 'X' on an output can indicate that an error has occurred as the signal has passed through the model.

'-' : This also represents a strong unknown and as such can be anything from a strong low to a strong high signal. This is sometimes referred to as NOT 'X'. It can provide a good logic level but it is a don't care state where its actual value is unimportant.

'W' : This state is a weak version of the 'X' data type noted above.

'L' : This data type represents a weak low, that is a low signal having a weak drive strength. This state can also represent a charge storage when used as an output state.

'H' : This is exactly the same as an 'L' however in the opposite sense, that is say it represents a weak high.

'0' : This is a strong low which can be input directly into a model.

'1' : This is a strong high and is the same as a 0 but in the opposite sense.

'Z' : This represents a high impedance signal and when used as an input it means nothing drives the node.

Referring back to the VHDL description of the invention, line 4 provides an arbitrary level to the design entity. This line starts the definition of a new VHDL design unit. Because the library and use clauses are written before the entity declaration they do not begin the VHDL description of the design unit, there are merely context clauses.

The entity declaration includes port declarations which are in lines 5 to 9. Ports may be pins on ICs or any other edge connection on a board etc. Technically ports are signals and so signals and ports are read in the same way. The port

**TABLE T.1**

The resistors R1 have the lowest resistance and are used to drive strong signals. The resistors R2 are used for the strong edge of the weak drive strength band. The resistors R4 have the highest resistance and are used to produce the very weakest signals.

In the following, R1 can have a resistance of 100Ohms, R2 a resistance 100K Ohms, R3 a resistance of 250 K Ohms and R4 a resistance of 1 MegaOhm. These values are by way of example only.

In Figure 3, resistor (R1) 302 is connected between high voltage supply rail VDD and the input to the analog model. This provides the strong 1 state to the analog model. Analogously resistor (R1) 303 is connected to the ground GND supply rail to supply strong 0 signals as inputs to the analog model. In this way inputs to the analog model which are identified as never changing state can be tied off to one of these inputs depending upon whether they are permanently strong high or low signals. This is provided by the first algorithm.

Resistor (R1) 304 is connected between a control input port 306 and the input to the hardware cell 301. By inputting a series of 0 and 1 signals as control signals on terminal 306 a series of strong 0 and 1 signals can be applied to the cell. This is provided by the second algorithm.

The following are used by the third algorithm. Signal generating circuits 308 and 309 each include a voltage control switch connected to a resistor R2. These resistors have an approximate value of 100kOhms. The circuit 308 is connected to the ground line whilst circuit 309 is connected to the high voltage supply line VDD. Each voltage controlled switch is operable in response to control signals input on control input terminals 310 and 311 respectively. The inputs on these